(12) UK Patent Application (19) GB (11) 2 221 570 (13) A

(43) Date of A publication 07.02.1990

(21) Application No 8818522.8

(22) Date of filing 04.08.1988

(51) INT CL⁴
H01L 21/58

(52) UK CL (Edition J)
H1K KPX K1BC K1EA K1EA1 K4C3G K4C3S K4C5A K4C5K K4C5M K5D9

(56) Documents cited
GB 2137131 A

(58) Field of search
UK CL (Edition J) B3R, H1K KPDA KPDB KPDC KPDX KPX
INT CL⁴ H01L

(71) Applicant
STC PLC

(Incorporated in the United Kingdom)

10 Maltravers Street, London, WC2R 3HA, United Kingdom

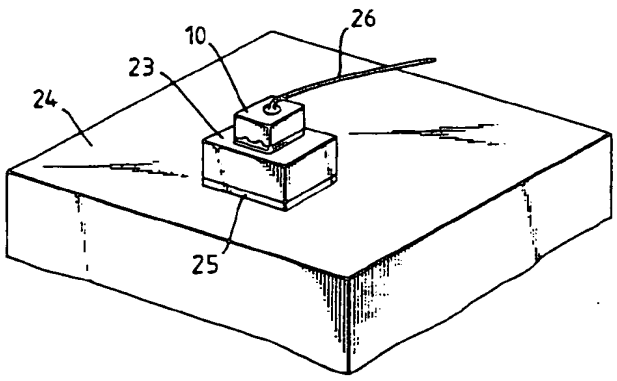
(72) Inventors
Arthur Walker
Peter Martin Bartholomew
Richard Fasching Murison

(74) Agent and/or Address for Service
S F Laurence
STC Patents, West Road, Harlow, Essex, CM20 2SH, United Kingdom

(54) Bonding a semiconductor to a heat sink

(57) A method of bonding a laser chip 10 to a gold coated diamond substrate 23 without the use of a discrete sold r preform involves metallizing the chip with a 2 to 3 μm thickness layer of tin sandwiched between submicron thickn ss layers of gold. Excess gold required for forming a substantially eutectic bond is taken up from a relatively thick coating of gold on the diamond substrate.

Fig. 2.



GB 2 221 570 A

At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy

2221570

Fig.1.

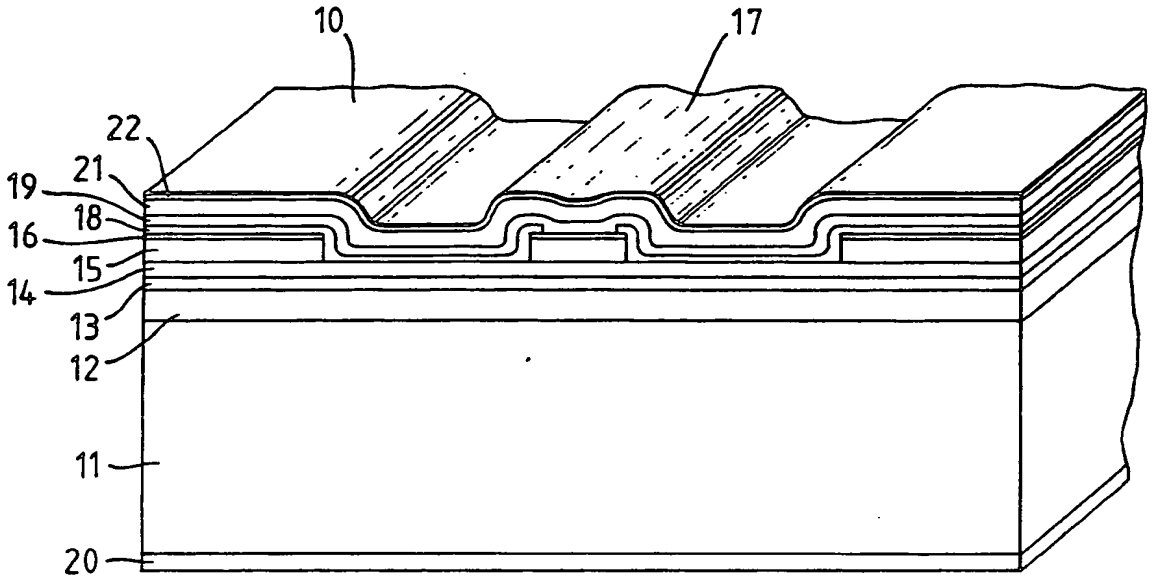
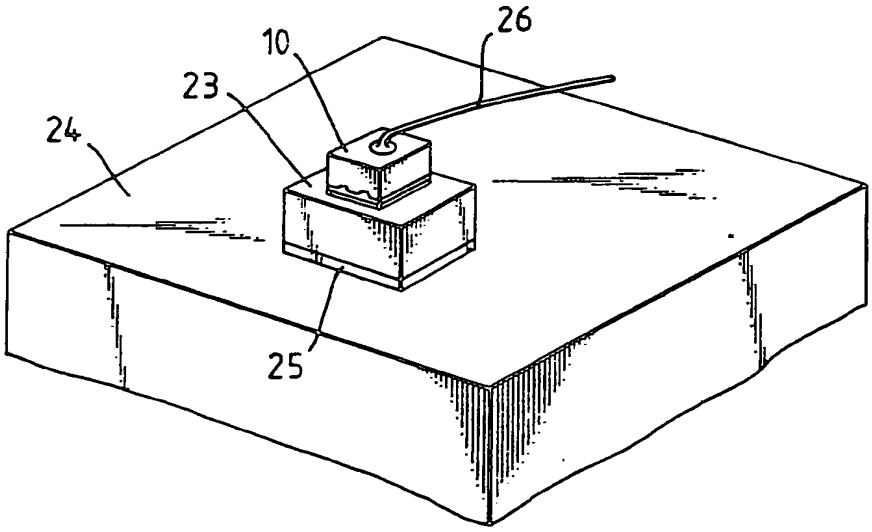


Fig.2.



LASER BONDING

This invention relates to the bonding of semiconductor bodies to substrates, and finds particular though not necessarily exclusive application in the mounting of injection lasers on heat sinks.

In a typical construction of InP/InGaAsP injection laser mount a laser chip is mounted on a gold-coated diamond substrate which in its turn has previously been mounted upon a copper heat sink. A gold germanium eutectic solder preform may be used for bonding the diamond substrate to the copper heat sink, and then a gold tin eutectic solder preform used for bonding the laser chip to the diamond taking care not to reach the melting point of the gold-germanium and thus risk disturbing the bonding of the diamond to the copper heat sink. The diamond provides a good thermal expansion match with the semiconductor chip as well as good thermal conductivity. The gold tin eutectic solder is resistant to void formation and whisker growth during the subsequent life of the laser, this being important both to retain low thermal impedance between the chip and the heat sink and to ensure that the laser is not short-circuited by whisker formation. Whisker formation appears to be associated with tin and tin-rich gold tin alloys, that is alloys incorporating phases which include more tin than gold on an atomic basis.

Although this bonding technique has been in commercial production for a number of years, we have found its implementation never to have been totally straightforward. The yeild of satisfactory devices has

relied heavily on the skill of the operator making the bond between the chip and the diamond substrate. The surface metallurgy of both substrate and chip appears crucial to the achieving of a successful bond. The use of a solder preform implies two pick-and-place operations per bond, and the geometry of the preform has to be carefully optimised for every size of chip. The flow and wetting of the chip and substrate by the solder is characterised by a phenomenon which can be characterised as 'suck-back'. The underlying physical processes involved in this phenomenon are not understood, but it appears that 'suck-back' is essential to the proper formation of the solder bond, and most problems associated with achieving satisfactory bonding are heralded by failure to achieve 'suck-back'. It is believed that 'suck-back' is caused by a change in surface tension forces produced when the solder wets both the chip and the substrate. Our investigations appear to show that the chip is wetted before the substrate, and that it is the substrate that is the single most important variable in determining the success rate in achieving satisfactory bonding.

In GB 2 137 131 B, to which attention is directed, there is described a method of diffusion assisted bonding which avoids the use of a gold-tin eutectic preform. According to this method the surfaces to be bonded of both the laser chip and the diamond substrate are each provided with a relatively thick coating of gold, typically 2μm thick, and then one of the thus coated surfaces is coated with a submicron thickness coating of tin which is itself covered with a further coating of gold to prevent oxidation of the underlying tin. The coated surfaces are held together and heated to cause the formation of a continuous molten gold-tin alloy layer which diffuses into the gold of the two gold layers. The two gold layers are deliberately made relatively thick in order that this diffusion

should not penetrate right through the thickness of either layer.

One particular drawback to this method of bonding described in GB 2 137 131 B lies in the fact that it calls for the provision of the relatively thick coating of gold upon the semiconductor chip. Typically the metallising of semiconductor laser chips of a semiconductor slice is performed before the slice and divided up into individual chips, but the presence of such a great thickness of gold interferes with the satisfactory cleaving of the chips, leading for instance to a propensity for the gold to become detached from the chips in the cleaving process.

According to the present invention there is provided a method of forming a bond between a surface of a semiconductor body and a surface of a thermally and electrically conductive substrate, wherein the surface of the semiconductive body is coated with a submicron thickness layer of gold, wherein the surface of the substrate is coated with a layer of gold, wherein at least one of the gold layers is coated with a layer of tin which is protected from oxidation by itself being coated with a submicron thickness antioxidant coating of gold, wherein the thickness of the gold layer on the substrate is sufficient for substantially all of said tin, when molten, to take up the gold and form a gold tin alloy substantially devoid of tin-rich phases, and wherein the two coated surfaces are held in contact while the resulting assembly is heated to a temperature sufficient to fuse said tin and cause the formation of said alloy which, upon subsequent cooling of the assembly, provides a bond between the semiconductive body and the substrate.

Particularly in the case of a semiconductor body which has a number of semiconductor layers grown epitaxially upon a semiconductor substrate, and which is to be bonded with those epitaxially grown layers facing

the thermally and electrically conductive substrate, a diffusion barrier layer coating, for instance of platinum or palladium, may be incorporated into the structure between the semiconductive material of the semiconductor body and the submicron thickness layer with which it is coated on the side to be bonded to the substrate.

Preferably the tin layer is a coating applied to the semiconductor body rather than to the substrate. This tin layer may typically be about 2 to 3μm in thickness. Such a thickness of tin is not found to present the cleaving problems that are found with a gold coatingof that thickness. A feature of the present invention is therefor that it is fully compatable with the conventional practice of semiconductor device manufacture in which metallisation is applied to a slice of chips before that slice is divided up into individual chips. In instances where the tin layer is a coating applied to the semiconductor body rather than to the substrate, another feature is that there is relatively little gold that the molten tin can take up in the bonding process prior to its wetting the substrate. This is advantageous because we have found that gold surface is more easily wetted by a tin-rich gold tin alloy than by gold tin eutectic or gold-rich gold tin alloy.

In contrast with the method of GB 1 137 131 B, this method of bonding of this invention does not involve any attempt to prevent the diffusion of the tin during the bonding process right through the whole depth of the gold layers between which it is sandwiched. The tin layer can therefore be made much thicker than as taught by GB 1 137 131 B. In the case of bonding InP/InGaAsP ridge waveguide structure laser chips ridge face-down on to supporting substrates a layer thickness typically in the range 2 to 3μm is preferred, this being sufficient to fill the channels extending down either

side of the ridge in the case of channels which in the completed chip are approximately 7μm wide and 2μm deep. The complete filling of these channels is advantageous in order to avoid the trapping of bubbles whose presence could seriously impair the rate of heat extraction from the chip.

There follows a description of the bonding of a ridge waveguide structure InP/InGaAsP laser to a substrate in a manner embodying the invention in a preferred form. The description refers to the accompanying drawings in which:

Figure 1 is a diagram depicting the structure of the ridge waveguide laser chip, and

Figure 2 depicts the chip of Figure 2 in position for bonding to a gold-coated diamond substrate that has itself been previously bonded to the surface of a copper heat sink.

Referring now to Figure 1 and InP/InGaAsP ridge waveguide structure laser indicated generally at 10 has an n^+-type indium phosphide (InP) substrate 11 upon which are grown a succession of layers 12 to 16 by liquid or vapour phase epitaxy. The first epitaxial layer to be grown, layer 12, is an n-type InP buffer layer, typically between 1 and 5μm in thickness. Its growth is succeeded by the growth of layer 13 which is the active layer of the device. The active layer is thinner, typically being in the range from 0.08μm to 0.50μm in thickness, and is made of p-type or n-type InGaAsp. Its composition is chosen having regard to the wavelength of emission required from the device. Layer 14 is a p-type anti-meltback/guide layer, also of quaternary InGaAsP, but of a composition corresponding to a shorter emission wavelength than that of the active layer. The thickness of layer 14 lies typically in the range 0.1 to 0.3 μm. The remaining epitaxial layers of the structure, layers 15 and 16, are respectively a p-type cladding layer of InP which is typically about

1.5 μm thick, and a p-type contact layer of InGaAsP which is typically about 0.2 μm thick and may conveniently have the same composition as that of layer 14. Wet chemical etching is employed to etch two channels through the contact and cladding layers 16 and 15 so as to define an intervening ridge 17 that is typically between 3 and 5 μm in width. These channels are etched through an oxide mask (not shown) after photolithography.

A layer 18 of silica to a depth of about 0.3 μm is deposited over the surface to provide electrical insulation, and then a window registering with the ridge is opened in this silica. Next the substrate 11 is thinned from about 300 μm to about 100 μm before the deposition of evaporated p-type contact metallisation 19 on the top surface and evaporated n-type contact metallisation 20 on the bottom surface. These metallisations are then alloyed in to the semiconductor material. In the case of layer 19 this alloying-in occurs only on the ridge 17 because elsewhere the silica insulation 18 acts as a mask.

For the p-type contact metallisation 19 there may be used a layer of titanium approximately 60 nm thick followed by a diffusion barrier layer of platinum approximately 200 nm thick followed, after alloying-in, by a layer of gold approximately 160 nm thick. For the n-type contact metallisation 20 there may be used a layer of gold-rich gold/tin alloy typically (4% Sn) approximately 140 nm thick followed, after alloying-in, by a layer of gold approximately 600 nm thick. The thicknesses of the gold layers of the p-type and n-type metallisations have been quoted for a chip that is to be bonded p-type side face-down on to its supporting substrate. Under these circumstances the n-type side gold layer is made as thick as is conveniently possible, consistent with being able to cleave the metallised chip from the slice, so as to facilitate the subsequent

making of a wire bonding contact with this n-type side of the chip.

For devices bonded n-type side face-down the thicknesses of the gold layers would be reversed, and the n-type metallisation may additionally include a diffusion barrier layer, for instance of platinum, between the gold rich tin and the gold. A gold germanium or gold germanium nickel alloy can for instance be substituted for the gold tin alloy for both p-side up mounted devices and p-side down ones.

Following metallisation of the laser chip, its surface to be bonded coated with a layer 21 of tin of between 2 and 3 μm in thickness, deposited by evaporation. This is immediately followed by the deposition, also by evaporation, of a gold layer 22 about 100 nm thick, which is provided to protect the surface of the underlying tin from oxidation. The chip is then ready for being separated from its neighbours in the semiconductor slice by cleaving.

Reffering now to Figure 2, the laser chip 10 of Figure 1 is to be bonded to a gold coated diamond substrate 23, which has itself been bonded to a copper heat sink 24. The bond of the substrate 23 to the heat sink is made using a gold germanium eutectic solder preform 25. The melting point of this eutectic is higher than that of the gold tin eutectic and so the bonding of the laser chip to the diamond substrate can be effected without disturbing the gold germanium eutectic bond.

In the case of a diamond substrate supplied with a 1 μm thickness layer of sputtered gold, this coating is thickened up to ensure sufficient gold is present for the bonding of the laser chip by depositing by evaporation a further 2 μm of gold on top of the 1 μm of sputtered gold.

After the bonding of the substrate 23 to the heat sink 24, the laser chip 10 is placed in position on

the substrate 23, and the assembly is heated up to about 300 to 320°C. The tin starts to melt at the relatively low temperature of 232°C. When this is noticed the chip may be lightly tapped with the collet (not shown) with which it has been positioned. This provides a mechanical initiation of the wetting of the gold of the substrate. This gold dissolves in the melt to form an alloy of approximately eutectic proportions at which time it appears that the wetting forces in the molten alloy abruptly change and "suck-back" occurs. At this point the bonding operation is terminated. The heating is turned off and the collet is removed clear of the chip. Typically the whole heating cycle takes no more than 30 seconds.

The layer thicknesses involved in forming the bond appear to be relatively flexible. These tin layers over the thickness range 2 to 3 μm work satisfactorily. With the thicker amount of tin it is clear that more gold needs to be taken up from the coating of gold on the substrate. If the thickness of this coating is not sufficient to permit all the necessary gold to be taken up from immediately beneath chip, the surplus tin is found to creep away from under the chip to take up the additionally required gold from the surrounding area.

The phase diagram of the gold tin system shows a solidus at 418°C corresponding to the 50:50 At % composition. This is considerably higher than the temperature employed to form the bond, about 300 to 320°C, which needs to be kept safely below the melting point of the gold germanium eutectic at 356°C so as to avoid the risk of disturbing the bond between the substrate 23 and the heat sink 24. Because this solder composition starts out as almost pure tin it was anticipated that the final alloy might include a number of tin-rich phases due to the limitations of the amount of gold dissolution imposed by the solidus. Such phases might prove susceptible to migration and whisker

formation and hence be unacceptable. Surprisingly metallographic analysis of the final alloy composition revealed it to be substantially identical throughout the whole thickness of the bond with that obtained when using an 80:20 Wt % eutectic solder preform.

The completed bond of the chip 10 to the substrate 23 provides one terminal connection for the chip. The other terminal connection is provided by a wire bonded lead 26.

Although the foregoing specific description has related exclusively to the bonding of laser chips to thermally and electrically conductive substrates, it is to be understood that the invention is applicable also to the bonding of semiconductor chips to non-conductive substrates. Thus for instance it is applicable also to the bonding of PIN diodes to ceramic substrates in constructions which are require to be free of epoxy resin.

CLAIMS

1. A method of forming a bond between a surface of a semiconductor body and a surface of a substrate, wherein the surface of the semiconductive body is coated with a submicron thickness layer of gold, wherein the surface of the substrate is coated with a layer of gold, wherein at least one of the gold layers is coated with a layer of tin which is protected from oxidation by itself being coated with a submicron thickness antioxidant coating of gold, wherein the thickness of the gold layer on the substrate is sufficient for substantially all of said tin, when molten, to take up the gold and form a gold tin alloy substantially devoid of tin-rich phases, and wherein the two coated surfaces are held in contact while the resulting assembly is heated to a temperature sufficient to fuse said tin and cause the formation of said alloy which, upon subsequent cooling of the assembly, provides a bond between the semiconductive body and the substrate.

2. A method as claimed in claim 1 wherein a diffusion barrier layer is applied to the surface of the semiconductor body prior to the coating with a submicron thickness layer of gold.

3. A method as claimed in claim 1 or 2 wherein only the gold layer of the semiconductor body is coated with a layer of tin.

4. A method as claimed in claim 3 wherein the layer of tin has a thickness lying in the range from 2 to 3 um.

5. A method as claimed in any preceding claim wherein the bonding of the semiconductor body to the substrate is preceded by the bonding of the substrate to a heat sink using a gold germanium eutectic solder.

6. A method as claimed in any preceding claim wherein the semiconductor body is an injection laser chip.

7. A method as claimed in claim 6 wherein the

injection laser chip is an InP/InGaAsP chip.

8. A method as claimed in claim 6 or 7 wherein the injection laser chip is a ridge waveguide structure laser.

9. A method as claimed in claim 6, 7 or 8 wherein the laser chip includes a semiconductor substrate supporting a plurality of epitaxially deposited semiconductor layers and wherein the semiconductor body is bonded to the substrate with the epitaxially deposited layers facing the bond.

10. A method of bonding a semiconductor body to a substrate which method is substantially as hereinbefore described with reference to the accompanying drawing.

11. An assembly including a semiconductor body bonded to a substrate by a method as claimed in any preceding claim.

)a: The Patent Office, State House, 66 71 High Holborn, London WC1R 4TP Further copies may be obtained from The Patent Office.
Sales Branch, St Mary Cray, Orpington, Kent BR5 3RD Printed by Multiplex techniques ltd, St Mary Cray, Kent, Con. 1/87